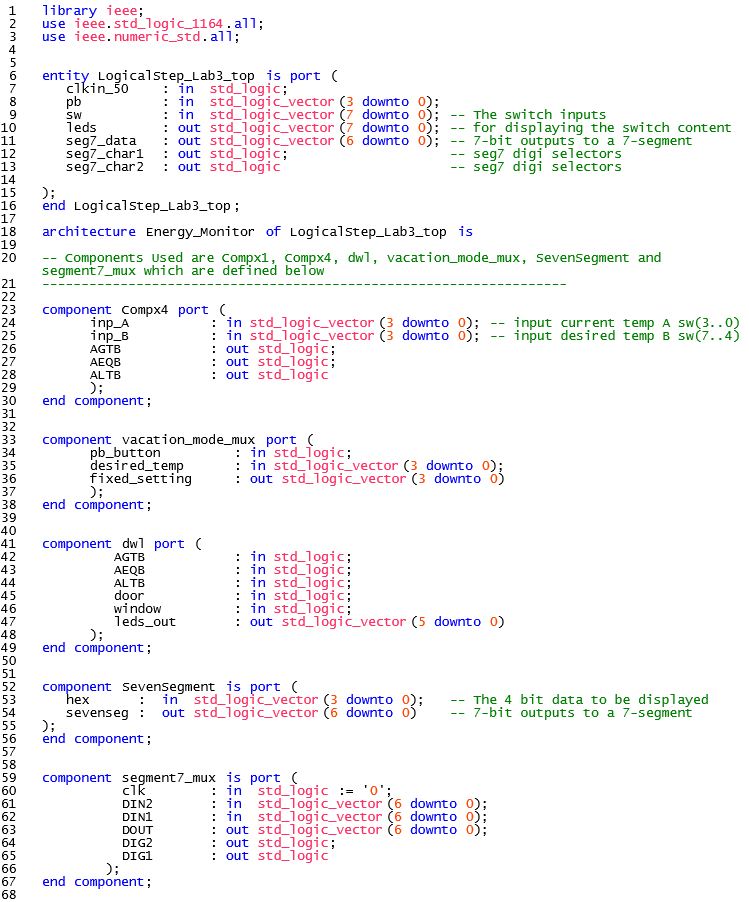
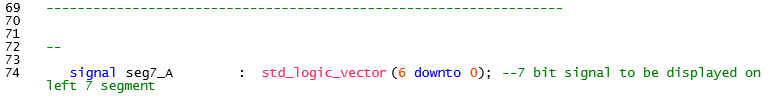
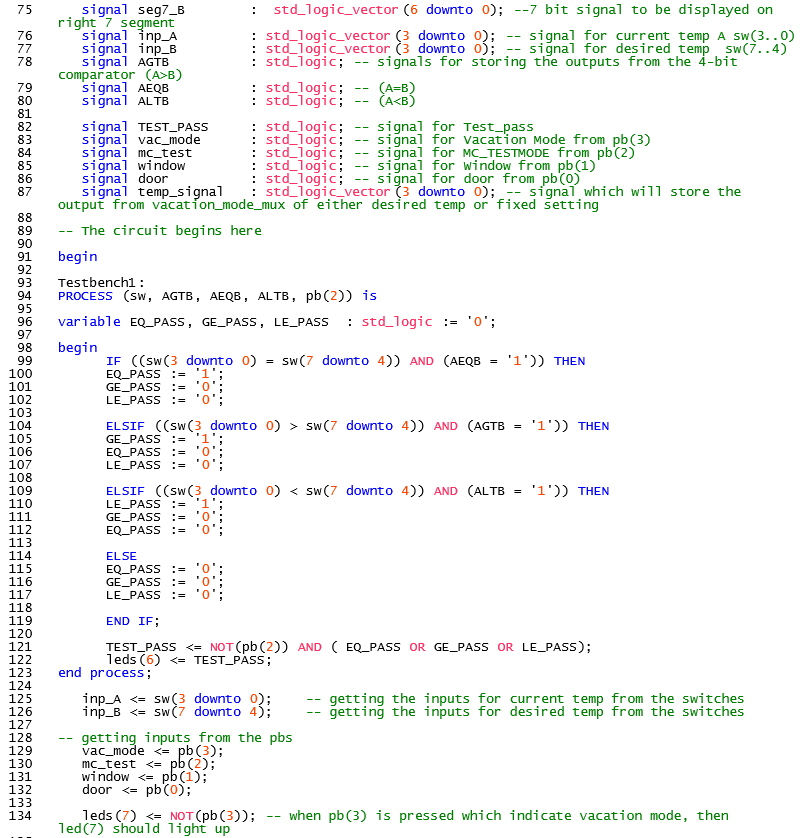
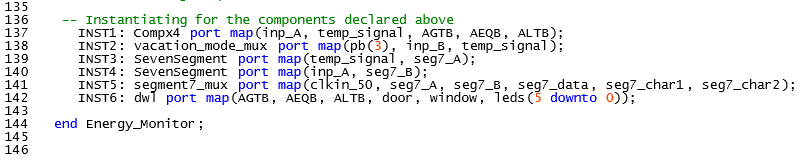
**Lab 3 Group 12 Session 205 Report**

**Part 1**: LogicalStep\_Lab3\_top.vhd File



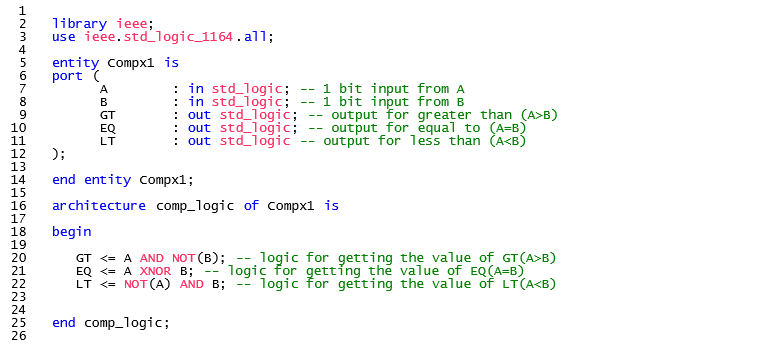




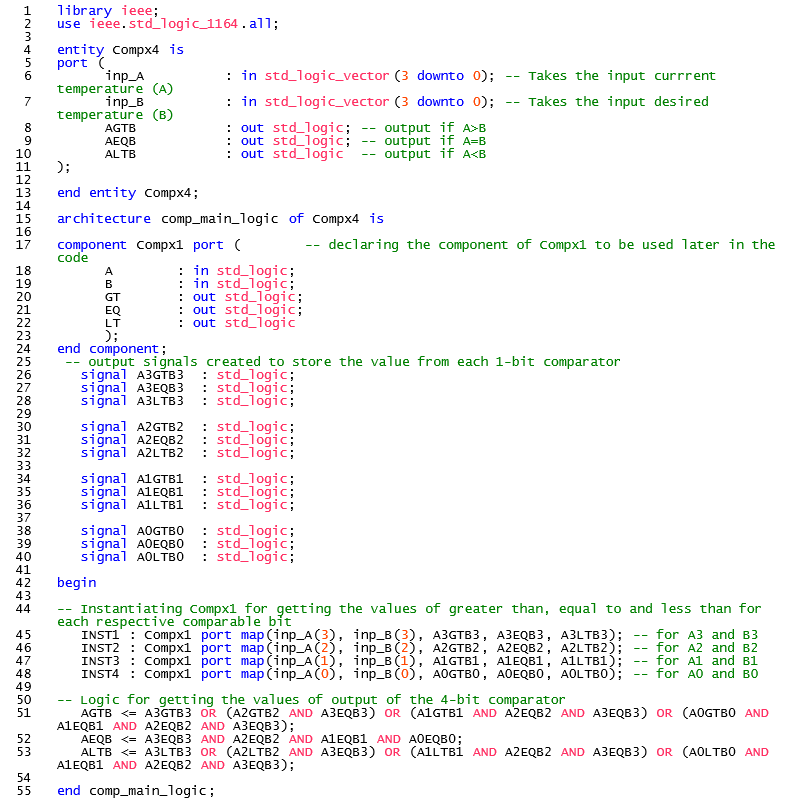


**Part 2**: Subordinate VHDL Files

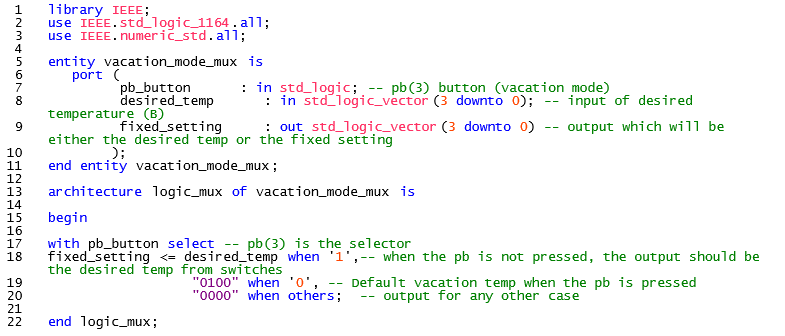
1. Compx1.vhd File



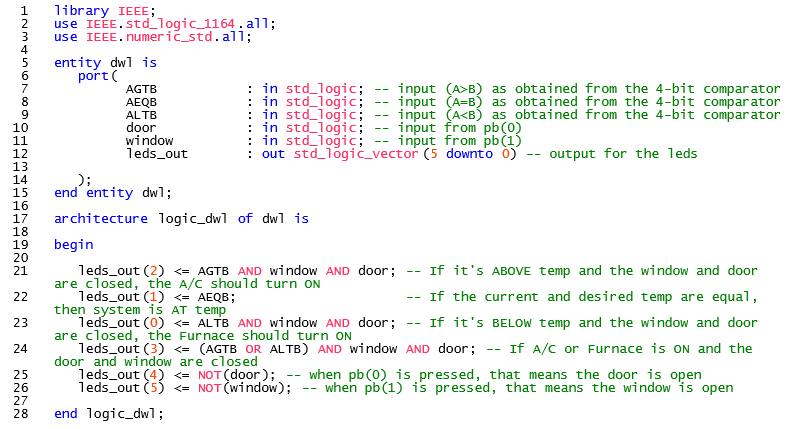
1. Compx4.vhd File



1. vacation\_mode\_mux.vhd File

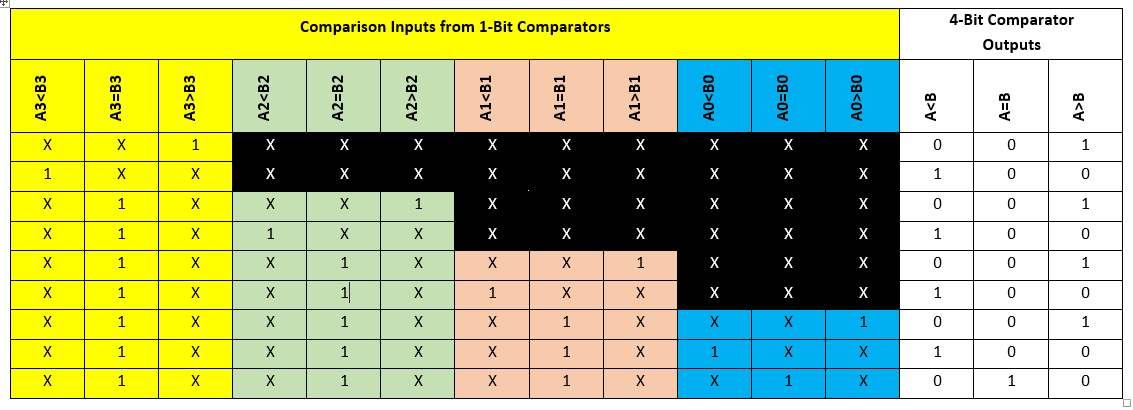


1. dwl.vhd File

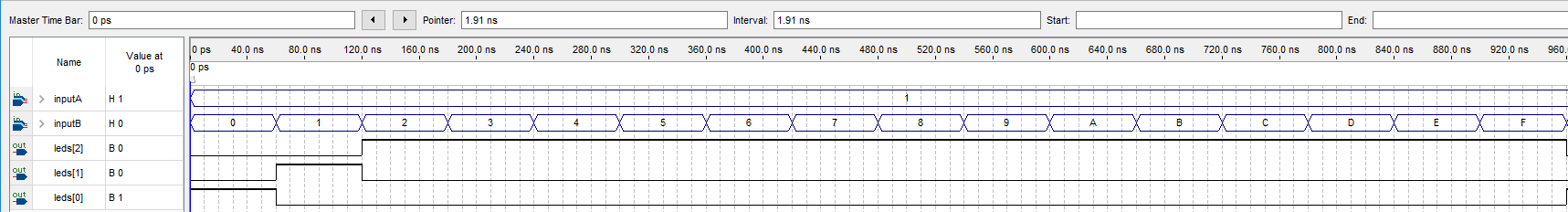


**Part 3:** Supporting Documentation

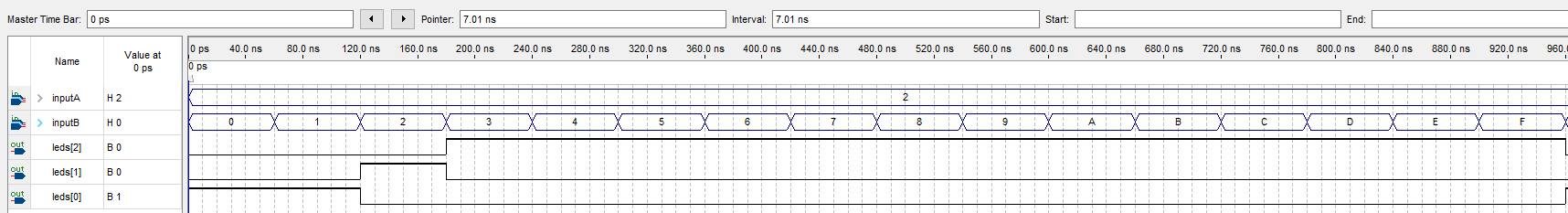
1. Truth Table



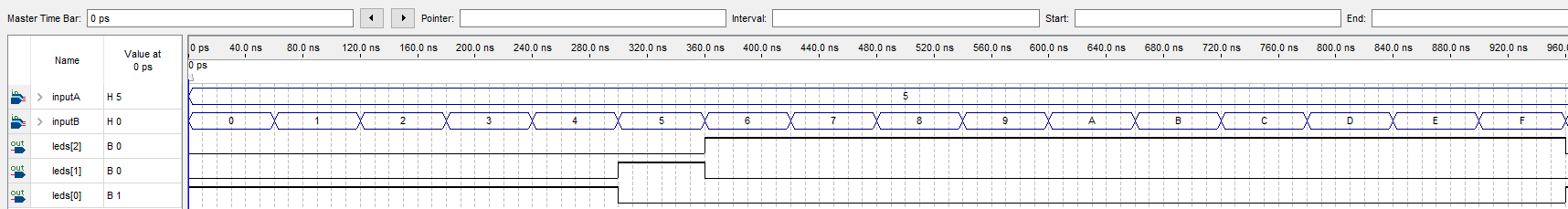
1. Simulations of Comparator



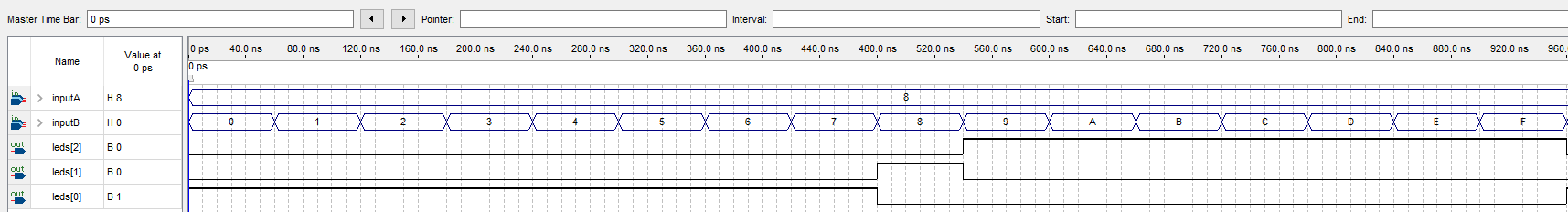
**Figure 1: Simulation 1 with Input\_A set to hex 1**



**Figure 2: Simulation 2 with Input\_A set to hex 2**

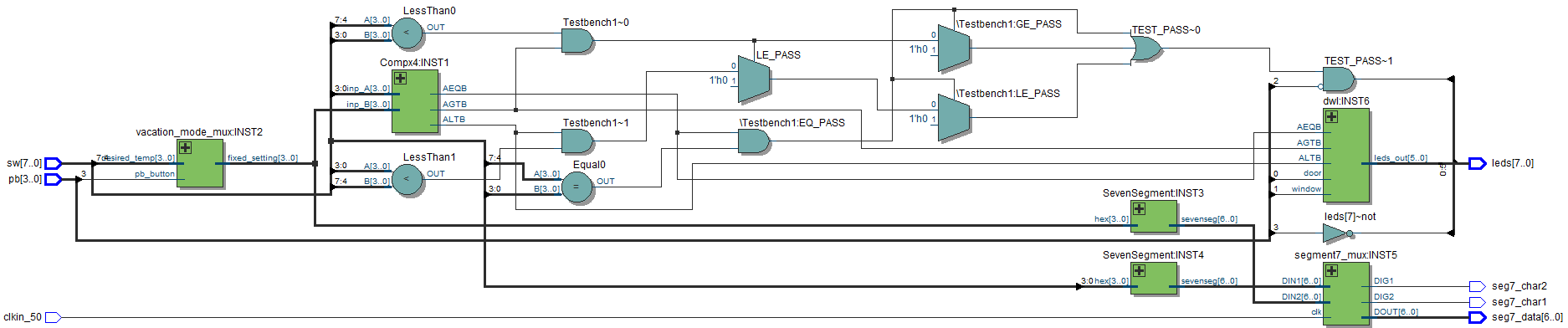


**Figure 3: Simulation 3 with Input\_A set to hex 5**



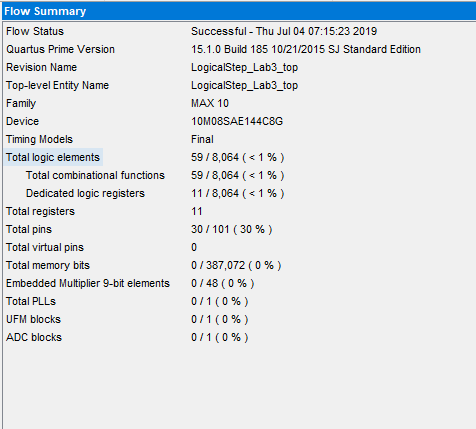
**Figure 4: Simulation 4 with Input\_A set to hex 8**

1. RTL View of the Logic Design (Top Level)



**Figure 5: RTL View**

1. Total Design Logic Elements Used: **59**



**Figure 6: Flow Summary**